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Quaternary 16X1 Multiplexer Design by using CMOS Multivalue Logic

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***Abstract* – The circuits design using CMOS logic with large number of transistotors and maximum length interconnect are gradually more prevailing contributor to propagation delay, overall area and power consumption. The circuits design using CMOS logic with large number of transistotors and maximum length interconnect are increasingly the dominant contributor to delay, area and energy consumption. The use of multivalue logic with a single voltage supply and employing only simple voltage mode structures. reduces the number of interconnections with carry more information on a one line . which in turn reduces the power consumption. In this paper the multivalue logic multiplexer and decoder circuit on 50nm technology is propose. The transmission gate is use for the design of 16X1 multivalue logic multiplexer circuit. The charging time of TG is proportional to its time constant, thus to enhance the speed of circuit the switching resistance is require to decrease. The circuit is companionable with standard CMOS base circuits.**

***Keywords* – MVL, Ternary Logic, Quaternary Logic, 16X1 multiplexer, Transmission Gate (TG).**

I. INTRODUCTION

The scaling of CMOS technology reduces the area of design with the optimization of design constraints such as speed, power etc. As CMOS come within reach of physical and technological limits, innovative devices have been proposed to design nanoscale circuits, such as those based on multiple-valued voltage level logic operations. Multiple valued logic (MVL) circuits with the three or four voltage levels are design at nanoscale range are advantageous in information density and operating speed. This paper provides a thorough assessment of several design constraints, such as static power consumption, switching power consumption, propagation delay and the power delay product (PDP).

The binary logic includes two voltage levels of 0V and 5V characterize as 0 and 1 in binary form. While the multivalue logic including of more than two voltages levels 0, 1, 2 for ternary logic and 0, 1, 2, 3 for quaternary logic. This gives more information on single line as compare to binary logic.

II. MULTIVALUE LOGIC

The ternary and quaternary binary number systems are mostly use in digital circuits. The number levels in these systems are: for ternary system it is 0,1,2 and for quaternary system it; is 0,1,2,3 numbers. The decimal equivalent numbers in ternary logic is 0,1,2,10,11,12,20, 21,22,30 for the decimal 0,1,2,3,4,5,6,7, 8,9 respectively and that of quternary is 0,1,2,3,10,11,12, 13,20,21 respectively. In this paper the multiplexer circuit for quaternary number system with 16 inputs and one outputs is design. For this the binary to voltage-mode standard CMOS circuits quaternary converter is use which convert the binary nubers to its quaternary equlivalent and use as inputs for 16X1 multipliplexer. The reference voltage use is of 5V and this voltage is deciminates in four levels for four quaternary numbers. These four levels of 0V, Vdd/2 V, Vdd/1.5 V and Vdd voltage level. The One quaternary variable is represented in binary form grouping two binary variables without information loss since the four quaternary level is represented by the four possible combination of two bit binary number. Hence the major advantage of quaternary logic is it gives more information on single line as compare to binary logic.

The relationship between decimal, binary, ternary and quaternary number system is shown in table 2.

Table 1: Decimal Number, Binary Number, Ternary Number, Quaternary Number.

Decimal	Binary	Ternary	Quaternary
0	0000	000	00
1	0001	001	01
2	0010	002	02
3	0011	010	03
4	0100	011	10
5	0101	012	11
6	0110	020	12
7	0111	021	13
8	1000	022	20
9	1001	100	21

III. DESIGN METHODOLOGY

In binary logic system the circuits work on two logic levels which logically represent '1' for true and '0' for false value. By difference, quaternary logic uses four voltage levels. Thus the logic gates such as AND, NAND, NOR, OR, etc., used for binary logics, cannot be work for quaternary systems. A transistor matrix circuit is use to design a binary to multivalue voltage levels. This transistor matrix is design using transmission gate logic.

The 2-bit binary to quaternary converter allows the use of a single row of switches to drive the input configuration signals to the output. The output is in the four voltage

levels of 0V, 1.5V, 3.0V and 5.0V. The purpose of design is to minimize number of gates needed and also to minimize depth of interconnect. Depth of interconnect is the largest number of gates in any path from input to output. The reason for choosing these two purpose is that they give optimizes design constraints when implemented in VLSI.

IV. MVL MULTIPLEXER

The fig 1 and Fig 2 shows the CMOS layout design of 4X1 multi value logic multiplexer and its timing simulation. The use of transmission gate reduces number of wires and routing capacitances. The charging time of transmission gate is proportional to time constant RC, hence to enhance the speed of circuit the switching resistance is decrease. The switching resistance of the NMOS and PMOS

Ronpmos = 1/uCoxW/L(Vgs – Vt)p

Ronnmos = 1/uCoxW/L (Vgs – Vt)n

Where,

u is mobility of charge carrier

Cox is oxide capacitance

W is channel width

L is channel length

Vgs is gate to source voltage

Vt is threshold voltage

The switching resistance of MOSFET is inversely proportional to channel width, thus to enhance the speed, it is need to decrease channel width. Also the switching resistance of transistor is inversely proportional to oxide capacitance thus increases in capacitance increases to a power to turn it on.

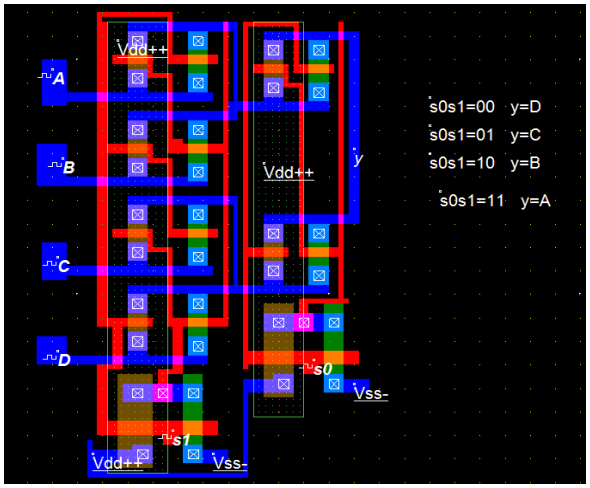

Fig.1. 4X1 MVL multiplexer.

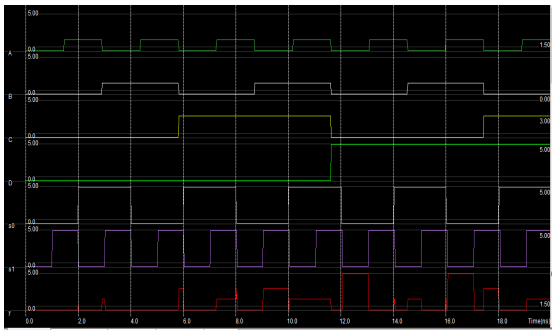

Fig.2. Timing Simulation of 4X1 MVL multiplexer.

The 4X1 MVL multiplexer is design with six transmission gate and one inverter circuit. It comprises of 14 MOS transistors.

Table 2: 4X1 MVL multiplexer truth table

Selection Line S0S1	4X1 Mux Output
00	D (0V, 5V)
01	C (0V, 1.3V)
10	B (0V, 1.5V)
11	A (0V, 1.5V)

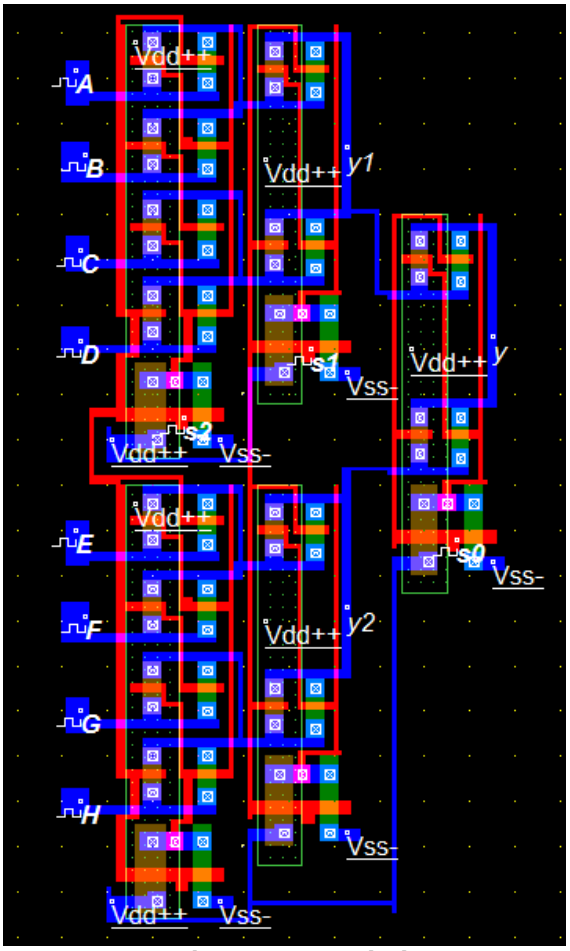

Fig.3. The 8X1 MVL Multiplexer

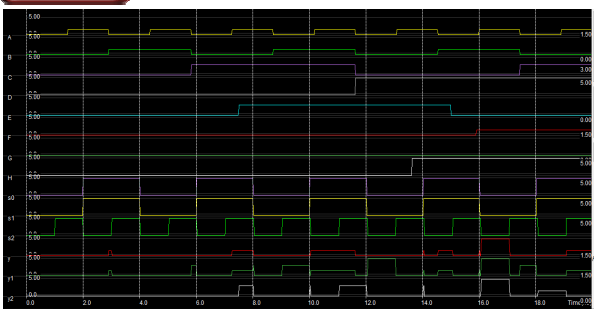

Fig.4. Timing Simulation of 8X1 MVL Multiplexer.

The 8X1 MVL multiplexer is design with fourteen transmission gate and five inverter circuit. It comprises of 38 MOS transistors.

Table 3: 8X1 MVL multiplexer truth table

Selection Line S0S1S2	4X1 Mux Output
000	D (0V, 5V)
001	C (0V, 1.3V)
010	B (0V, 1.5V)
011	A (0V, 1.5V)
100	H (0V, 5V)
101	G (1.5V, 3.0V)
110	F (0V, 1.5V)
111	E (0V, 3.0V)

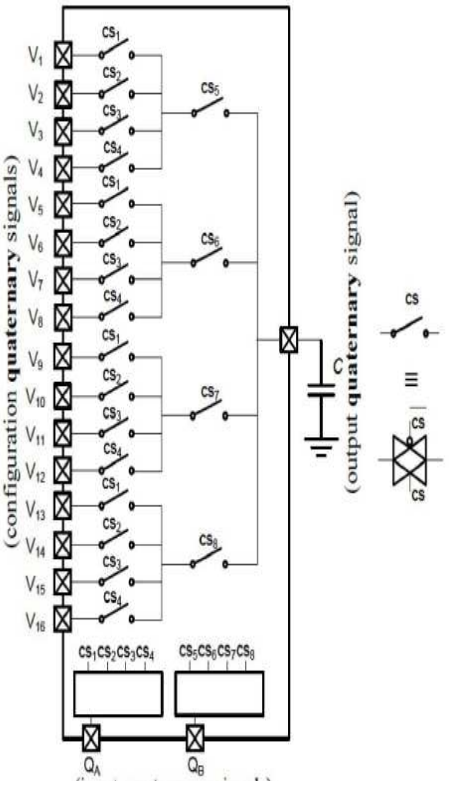

Fig.5. Transmission gate base Quaternary 16X1 multiplexer.

The multiplexer truth table for quaternary logic is shown in table 1.

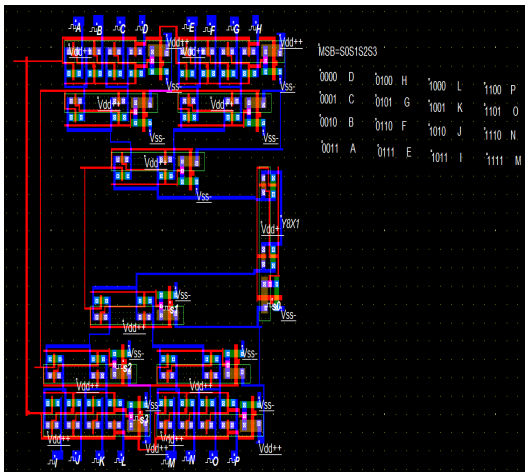

Fig.6. MVL 16X1 Multiplexer

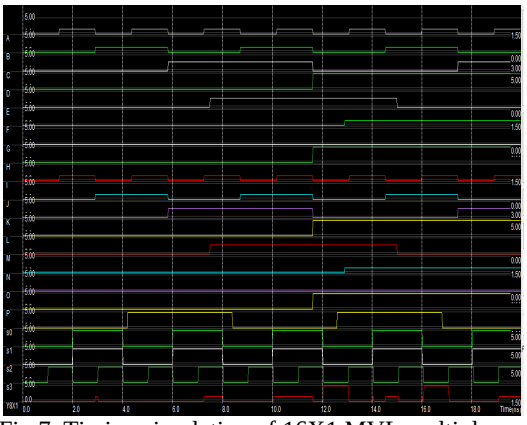

Fig.7. Timing simulation of 16X1 MVL multiplexer

The 16X1 MVL multiplexer is design with 42 transmission gate and 11 inverter circuits.

Table 4: Truth Table for 16X1 Quaternary 16X1 multiplexer.

Qa	Qb	Vout
0	0	D (0V,1.5V,3.0V 5V)
0	1	C (0V, 5V)
0	2	B (0V, 1.5V)
0	3	A (0V, 5V)
1	0	H (0V,1.5V,3.0V 5V)
1	1	G (0V,1.5V,3.0V 5V)
1	2	F(0V,1.5V,3.0V 5V)
1	3	E (0V, 3.0V)
2	0	L (0V, 1.5V)
2	1	K (0V, 5V)
2	2	J (0V, 3.0V)
2	3	I (0V, 1.5V)
3	0	P (0V, 1.5V)
3	1	O (0V, 1.5V)
3	2	N (0V, 3.0V)
3	3	M (0V, 1.5V)

Table 5: The parametric Analysis for Quaternary 16X1 multiplexer.

Parameters	**[1]**	**This Work (16X1)**
Technology	130nm	50nm
Supply Voltage	1.2V	5.0V
Switching Delay	4.4ns (1.5ns)	0.05ns (0.02ns)
Output Load	10pF	18pF
Transistor Count	220	82
Power Consuption	140uW	232uW

V. CONCLUSION

Multiple-valued logic has many theoretical advantages - its potential to increase the functional density of metal-limited digital integrated circuit layouts by reducing the number of signal interconnections We can design the multivalue logic to binary converter which is use for conversion of ternary-valued input 0,1,2 and quaternary-valued input 0,1,2,3 into corresponding binary-valued output 0,1. The physical design of the circuits is simulated and tested with MICROWIND layout design tool in 50nm technology. The conversion method is simple and compatible with the present CMOS process. The circuits could be embedded in digital CMOS VLSI design architectures. The Power consumption is calculates in the range of 232uW with the switching delay in the range of 0.02ns. The power dissipation is increase as compare to related work, but it optimize power dissipation in comparision with supply voltage of the circuit.

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