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# Parametric Optimization of Clocked Redundant Flip-Flop Using Transmission Gate

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***Abstract -- In this paper the flip-flops circuits are designed with adaptive coupled transmission gate working on conditional precharge and the conditional capture technologies so as to reduce the redundant switching activities. The schematic level circuits are design and the parametric optimization is done at layout level. The D flip-flops in digital integrated circuit consume 50 % of area and power due to the redundant transition at the internal nodes when the input and output are at the same state. Timing simulation of transmission gate based flip flop shows the best power and delay optimization. The layout is designed using Microwind layout with 0.05 µm technology. In this paper NAND latch and Flip-flop both are discussed, also D-Flip-flops are using transmission gates are explained.***

***Keywords*** **-- Transmission Gate, Master-Slave Latch, Adaptive Couple, Short Channel Effects, Flip-flops.**

## INTRODUCTION

To protect Flip-Flops (FF) from soft errors caused by short channel effects and to optimize power dissipation at high temperature field Adaptive Coupled (AC) Transmission Gate (TG) based circuit is used. Memory cells or latches are flipped if some amount of charge is generated due to particle hits. To reduce soft error rates, various redundant flip-flop structures are proposed [1,2].

The pass transistor used between master and slave latch creates the problem. As the PMOS pass transistor generates weak '0', output across load capacitor does not fully discharge the PMOS transistor. This creates a problem to pass strong '0' signal towards the slave latch from master latch. Thus, a positive edge triggered flip-flop structure is proposed in this work using AC transmission gates instated of pass transistor. The circuit is designed by using three cross connected transistor base latches using transmission gates. The major advantage of transmission gate is it minimizes the number of transistors required for design and stray capacitances form in the circuits due to CMOS structure and interconnects.

**The Cross Connected NAND Gate Flip-flop**

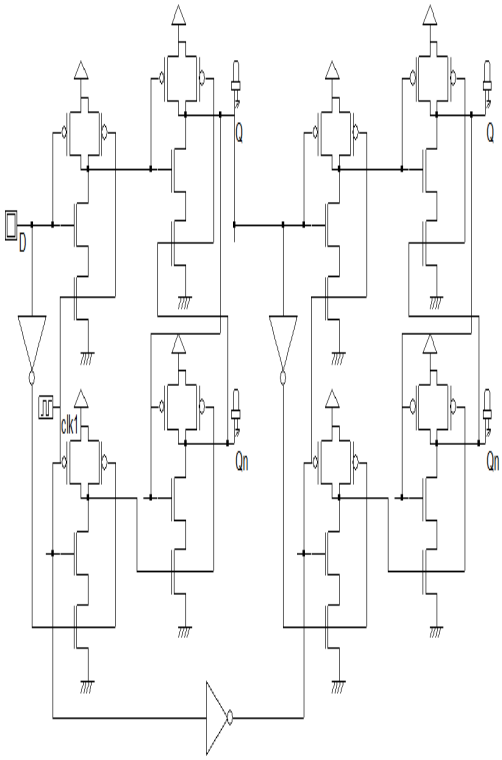


**Fig. 1 CMOS Schematic for Master Slave for Cross Connected NAND Latch**

The cross connected flip-flop with master and slave latch shown in fig 1 comprises of eight NAND gates. The CMOS schematic for NAND gate is designed with 2 NMOS and 2 PMOS transistors. Thus master slave flip flop is designed with 18 NMOS and 18 PMOS transistors with an inverter connected in the path of clock signal. The problem with master slave flip flop is it uses a level triggered latch i.e. it responds to a change in the level of a clock pulse. A positive level response in the enable input allows changes in the output when the D input changes while the clock pulse stays at logic 1. For proper operation of flip-flop the clock trigger only during a signal transition. This can be done by eliminating the feedback

path that is intrinsic in the operation of the sequential circuit using latches. The clock pulse use is either positive edge trigger i.e. from 0 to 1 or negative edge triggered i.e. from 1 to 0. One way is to use two latches in a particular design that separate the output of the flip-flop and avoid it from being affected at the same time as the input to the flip-flop is changing. A different way is to construct a flip-flop that triggers only during (see fig.3) a signal change either positive or negative edge of the synchronization signal and is disabled during the rest time duration of the clock signal pulse.

## II. METHODOLOGY

Flip-flop operates with the single-phase clocking scheme using pass-transistors. Without using local clock buffers, power dissipation can be reduced. As data activity becomes low, total power dissipation is drastically reduced. However, PMOS pass-transistors are too weak to pass through a substantially large drain current. It is difficult to overwrite the master latch because PMOS pass-transistors are located in front of the master latch. The Adaptive-Coupled (AC) two transistors make it easy to overwrite the master latch. When the next value is same as the current value, the cross-coupled loop keeps the current value. When it is different, the AC makes the holding value weak. Our goal is to trade off between these limitations and thus propose new methods which reduce both leakage and dynamic power with minimum possible area and delay trade off.

*Transmission Gate Adaptive Coupled D Flip-flop*

The functional description of master slave flip flop makes two observations that are: The change in output for one clock pulse duration is only once, and the change in input can affect the output at negative edge of clock pulse. At the positive level of clock pulse the output of master latch change according to the truth table of flip flop and at the negative edge of clock pulse this output of master latch is transfer to the output of slave latch. To design the positive edge trigger flip flop, a slight change in structure is made. Table 1 takes place in a FF by inserting a inverter between the Clk terminal and the junction between the other inverter and input En of the master latch. Such a flip-flop is triggered with a negative pulse, so that the negative edge of the clock affects the master and the positive edge affects the slave and the output terminal [3,4].

The fig 2 shows three latches to form the edge trigger flip-flop. This includes 14 transmission gates and 12 inverters. Total number of transistors requires to design this circuit is 52 transistors. The S and R inputs of the output latch are maintained at the logic-1 level when Clk = 0. This causes the output to remain in

its present state. Input D may be equal to 0 or 1. If D = 0 when Clk becomes 1, R changes to 0. This causes the flip-flop to go to the reset state, making Q = 0. If there is a change in the D input while Clk = 1, terminal R remains at 0 because Q is 0. Thus, the flip-flop is locked out and is unresponsive to further changes in the input. When the clock returns to 0, R goes to 1, placing the output latch in the quiescent condition without changing the output. Similarly, if D = 1 when Clk goes from 0 to 1, S changes to 0. This causes the circuit to go to the set state, making Q = 1. Any change in D while Clk = 1 does not affect the output [3,4,5,6].

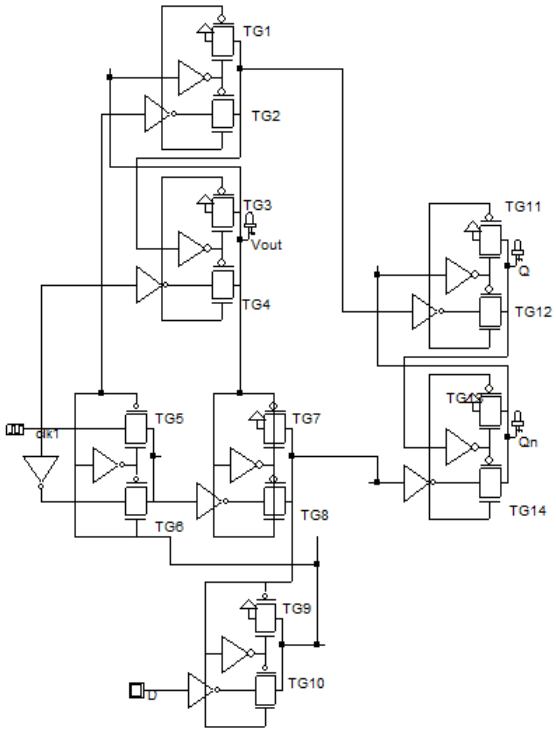


**Fig. 2 Proposed Edge Trigger D Flip-flop with Adaptive Coupled Transmission Gate**

When the input clock in the positive-edge-triggered flip-flop makes a positive transition, the value of D is transferred to Q. A negative transition of the clock (i.e., from 1 to 0) does not affect the output, nor is the output affected by changes in D when Clk is in the steady logic-1 level or the logic-0 level. The CMOS layout of edge trigger master slave latch design with 2 level trigger latch comprise of 4 NAND gates and 1 NOT gates each.In Fig.3 total numbers of transistors used are 38. The channel length of both NMOS and PMOS is 0.05 μm. The channel

width is 0.1 µm for NMOS and that of 0.3 µm for PMOS transistor. The total channel area is 1.9 µm².

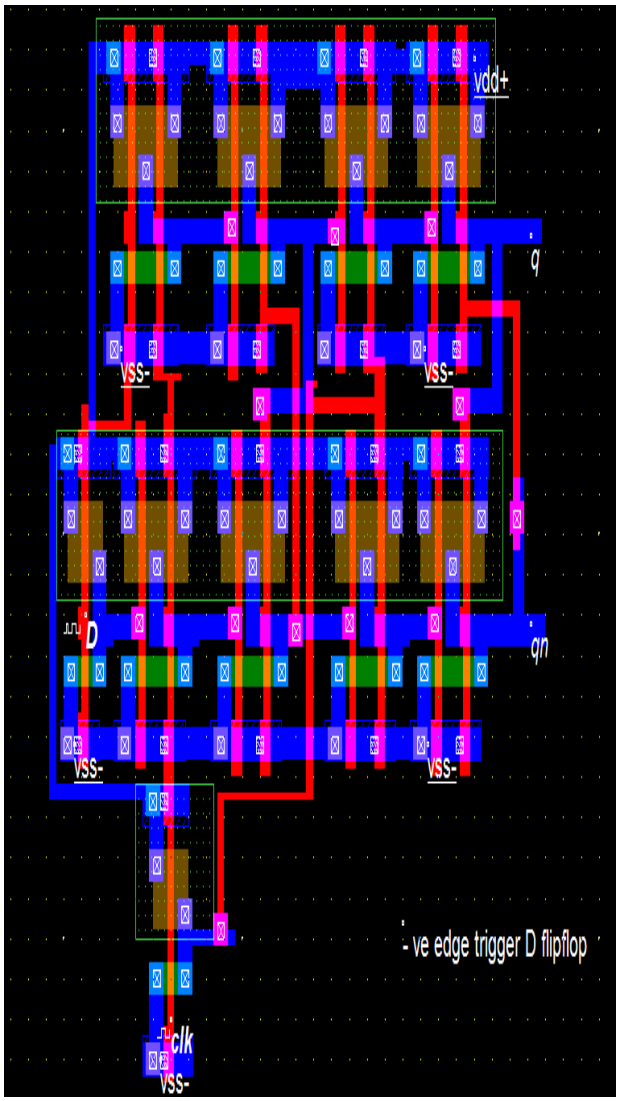


**Fig. 3 CMOS Layout for Master Slave Base D Flip-flop**

The fig 4 shows the timing simulation of edge trigger master slave latch. The change in input can affect the output at discrete instant of time depends on the behavior of the clock signal. Fig.5 shows layout of edge trigger master slave transmission gate based latch design with 3 level trigger TG Latch. In fig.5 total number of transistors are used 54.From table 2 the channel length of both NMOS and PMOS is 0.05$\mu$m. The channel width is 0.125 $\mu$m for both NMOS and PMOS transistor. The total channel area is 2.7$\mu$m².

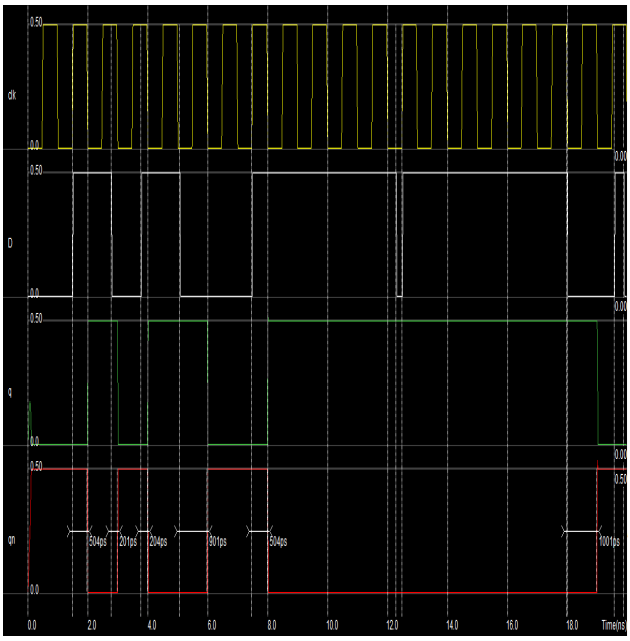


**Fig. 4 Timing Simulation of CMOS Layout for Master Slave Base D Flip-flop**

**Table 1**
**Parametric Analysis**

| Design Module | Tech-nology | Number of Transistor | Channel Area ($\mu$m²) | Power ($\mu$W) | Delay (ns) |
|---|---|---|---|---|---|
| NAND Latch | 50nm | 18 | 0.9 | 0.04 | 0.003 |
| Master slave latch | 50nm | 38 | 1.9 | 0.6 | 0.002 |
| **TG D latch** | **50nm** | **10** | **0.5** | **0.23** | **0.001** |
| **TG D master slave** | **50nm** | **23** | **1.15** | **0.5** | **0.006** |
| **Proposed TG D master slave** | **50nm** | **54** | **2.7** | **0.6** | **0.007** |
| **P TG T master slave** | **50nm** | **54** | **2.7** | **0.6** | **0.007** |
| **P TG JK master slave** | **50nm** | **72** | **3.6** | **0.8** | **0.08** |
| [1] BCDMR ACFF | 65nm | 62 | 2.84 | 2.21 | 1.27 |
| [1] BCDMR ACFF | 65nm | 56 | 3.16 | 1.16 | 1.11 |

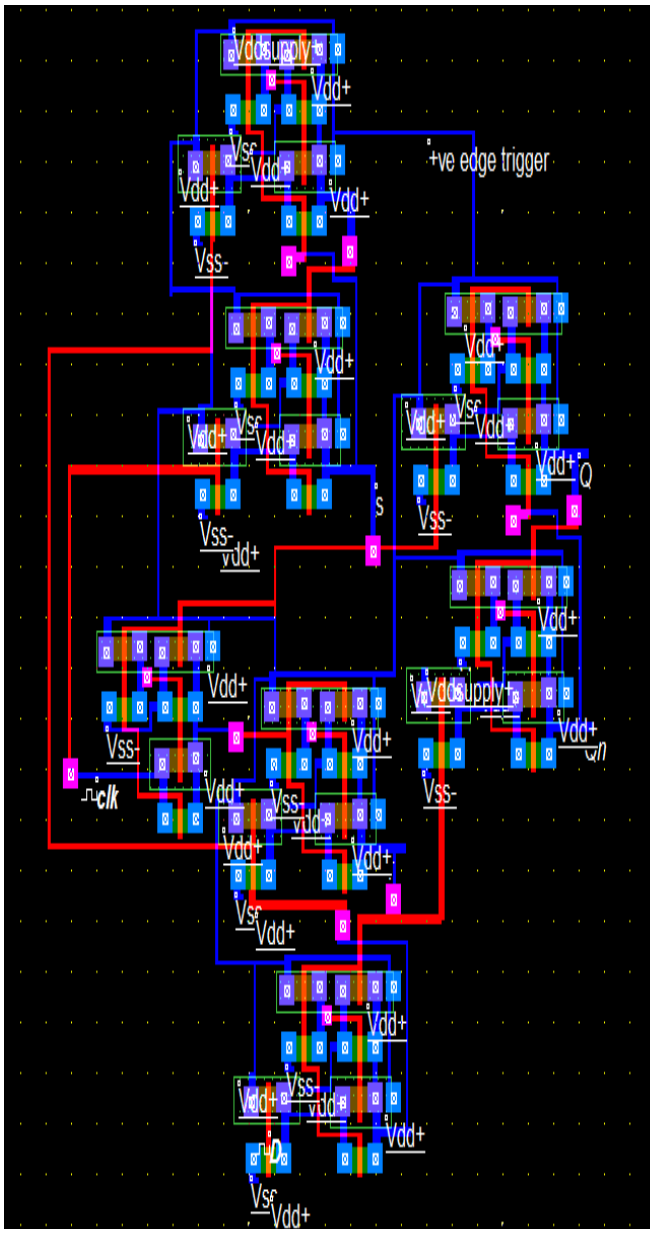


**Fig. 5 CMOS Layout for Edge Trigger D Flip-flop**

**Table 2**
**Calculation of Suitable Parameters for Edge Trigger D Flip-flop**

| Clk | D in | Q Out | Number of Transistor | Output Load | Power Dissipation | Delay |
|---|---|---|---|---|---|---|
| 1-0 | X | No Change | 54 | 0.57fF | 0.6uW | 0.007 ns |
| 0-1 | 0 | 0 | | | | |
| 0-1 | 1 | 1 | | | | |

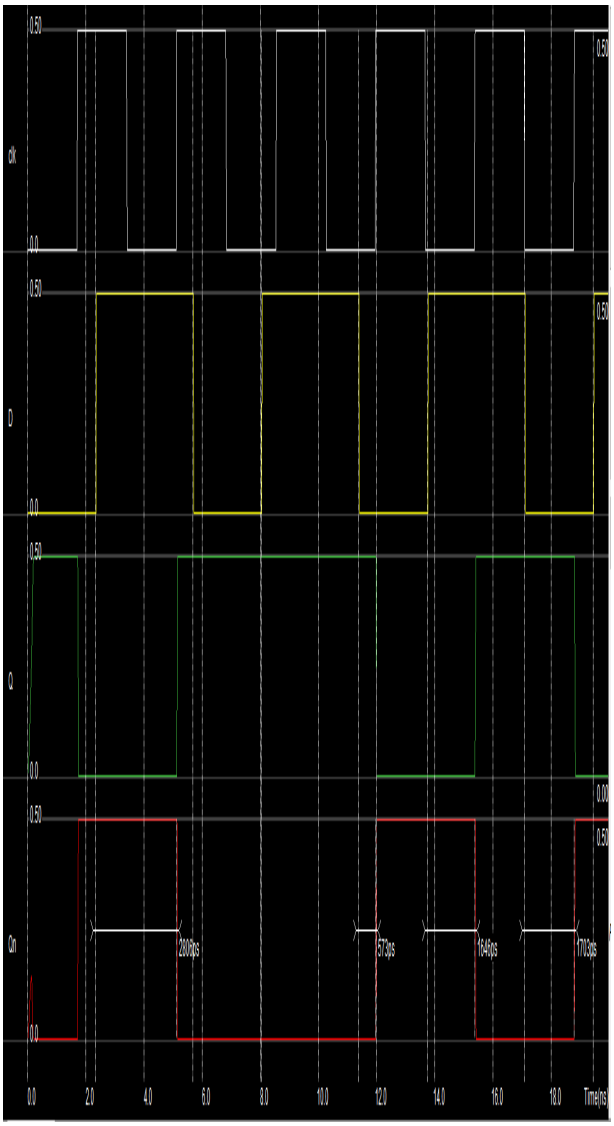


**Fig. 6 Timing Simulation of Edge Trigger D Flip-flop**

Fig 6 shows the timing simulation of proposed Edge Trigger D Flip flop. The parametric analysis is shown in Table 3, design module, delay, power dissipation, Number of transistor, channel area is discussed.

**Table 3**
**Calculation of Suitable Parameters for D Flip-flop**

| Clk | D in | Q Out | Number of Transistor | Output Load | Power Dissipation | Delay |
|---|---|---|---|---|---|---|
| 0 | X | No Change | 38 | 0.35fF | 0.6uW | 0.002ns |
| 1 | 0 | 0 | | | | |
| 1 | 1 | 1 | | | | |

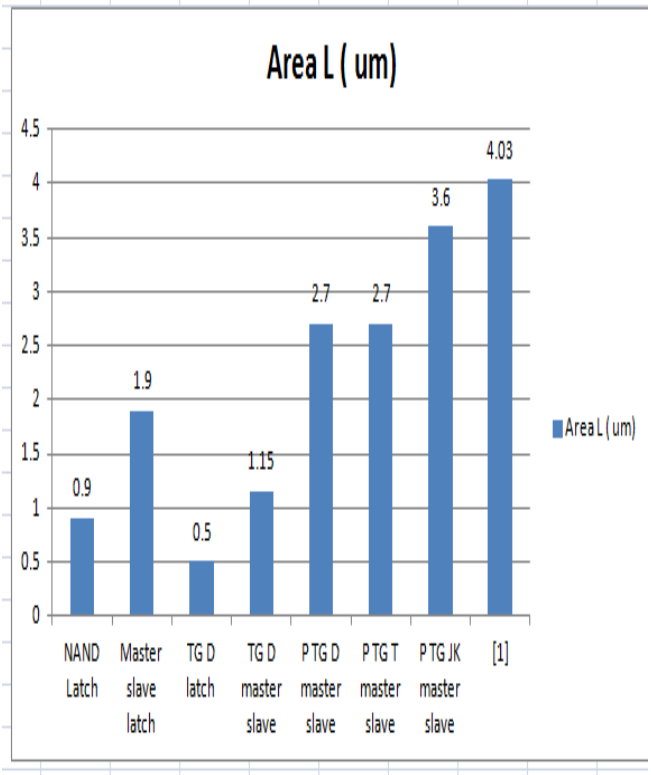


**Fig. 7 Graphical Analysis of area**

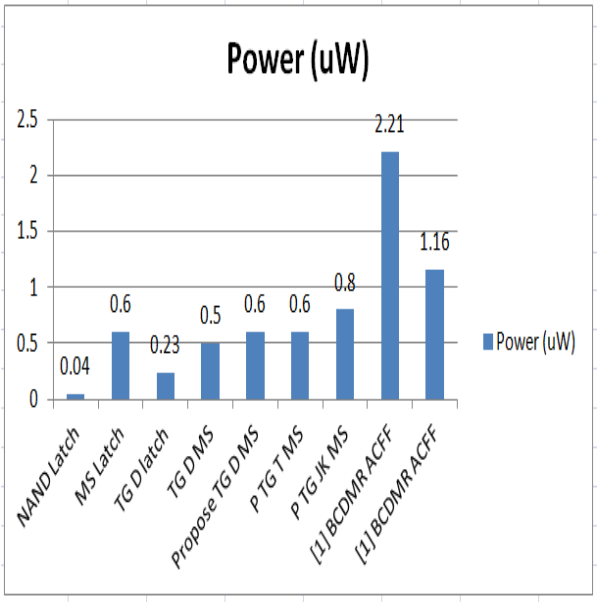


**Fig. 8 Graphical Analysis of Power Dissipation**

## III Conclusion

In this work we have discussed the schematic structure and operation for various flip-flops with its timing simulation. The transmission gate-based flip-flops exhibit the best power-performance trade-off with a total delay (clock-to-output) reduces as compare to conventional flip-flops. The use of transmission gate in FF design will reduce the number of transistors requirement and will also reduce the stray capacitances. In fig.7 the area is varied which is shown in proposed work area is reduced as compare to BCDMR. And From fig.8 Power dissipation is reduced in proposed work as compare to BCDMR ACFF.

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