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CMOS Voltage Reference Amplifier Design with Charge-Pump Circuit

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***Abstract* – The sub-threshold CMOS voltage reference circuit is fabricates using a 50nm technology. Voltage reference circuit with minimum supply voltage is design by replacing the Analog amplifier in the conventional CMOS voltage reference circuit with a low-voltage comparator, a charge-pump circuit, and a digital control circuit. A charge pump circuit is design with three state level. The charge pump circuit either charges or discharges a capacitor with voltage or current pulses**.

***Keywords* – Voltage Reference Amplifier, Charge Pump Circuit, Voltage Control Oscillator (VCO), Phase Lock Loop (PLL), Micro Wind.**

I. INTRODUCTION

The architecture was mostly studies in analog & digital design environment from MICROWIND. The simulation studies reveal the behaviour of the individual components which were found to be as expected. The fundamental difficulty of PLL design using deep submicron technology is to achieve low power consumption which may due to uncertainty in the value of threshold or supply voltage. Since PLLs are widely used in communication application such as frequency synthesis for missile tracking, noise stability is an important factor which can be analysed with the components of filter. When we add charge pump circuit between LPF and phase detector it will give more stable output. The Software used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. The electric extraction of our circuit is automatically performed and the analog simulator produces voltage and current curves immediately. This PLL circuit shows the variation of power consumption with supply variation & delay increases with temperature.

In portable devices like cell phones and other mobile devices, the system power supply voltage should be stable and should not be affected by discharging the battery input voltage. In the unregulated charge pump, the output voltage follows input voltage and is always a multiple of input. Such behaviour of the output voltage is not desirable in mobile phone devices. To maintain the output voltage at a stable value, several regulation schemes have been implemented. The most commonly used regulation methods involve current regulation, voltage regulation, and frequency regulation. The very-large-scale integration (VLSI) circuits with voltage battery backup circuit are mostly required in portable devices. These circuits need voltage reference circuits to provide precise and stable voltage signals. The required circuit have been implemented such that it operates at low voltage which should be below threshold voltage.

II. CHARGE PUMP CIRCUIT

The architecture of the proposed charge pump is based on continuous current pumping technique. In general, a charge pump is required to provide the load current, all the time. The input power supply should deliver enough charge during each clock cycle to fulfil the load current requirement. A typical charge pump has two clocking phases: 1) Charge phase – during which the charge is transferred to the load capacitor. 2) Discharge phase – during which the charge pump stops pumping charge. The load current is provided by discharging the load capacitor during the discharge phase. In the proposed architecture, the energy required to be delivered to the load is continuously provided by either the top half or the bottom half of the charge pump to the load capacitor. During a full cycle of the clock signal, there is no explicit discharge phase for the load capacitor. However, the load capacitor discharges a small amount of charge to fulfil the load current requirement during each half cycle which results in the output ripple voltage.

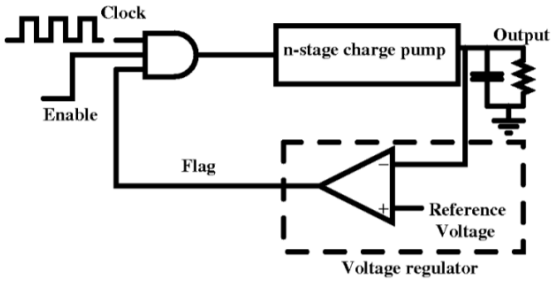

Fig.1. Basic Charge Pump Logic.

III. LOW VOLTAGE COMPARATOR

A two-stage CMOS op-amp is used in this ADC, as it is one of the most widely used and best understood op-amps. The core of the operational amplifier is the differential amplifier, so the chosen circuit layout is very influential

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on the overall performance of the op-amp. The technology employed is UMC 0.12 mm which consists of a p-substrate. Therefore a p-channel diff amp similar to that in fig was chosen. The reason for this is that a PMOS created using a p-substrate is more insensitive to bulk effects than an equivalent NMOS. If the situation was converse to this then an n-channel diff amp would be better suited. The bulk effect varies the MOSFET threshold voltage VT and occurs when the substrate voltage of the transistor is not the same as the source voltage. When this occurs the problem is that the polarity of the PN junction that exists between the bulk and the source can be altered. If it becomes forward biased then the transistor doesn't function properly. If it remains reverse biased the depletion region increases. A larger depletion region means that a larger charge will have to be applied to overcome it. Hence VT has increased. To eliminate this bulk effect in the differential transistors, PMOSs are used, so the situation can't arise where the junction between the source and the bulk is forward biased.

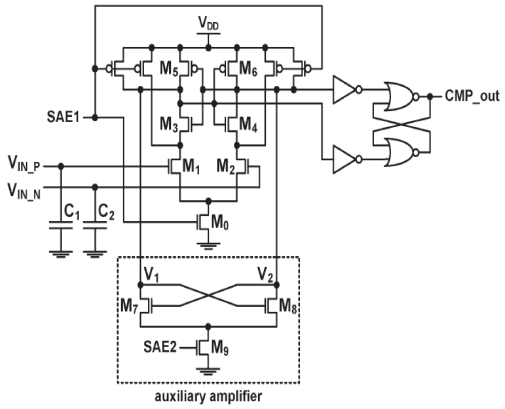

Fig.2. Op-amp as a Comparator

The higher the op-amps gain the more linear the ramp will be. The gain of the two stage op-amp is determined by both the gain of the diff amp stage and output stage. The first stage gain is given by $A_v = g_m (R_{on})$. The speed at which the differential amp can operate at is directly related to its slew rate. The slew rate of the differential amplifier is dependent on the value of the current ISS (which is determined by the current source) and also the capacitance from the output node to ac ground. Basically it can be expressed as:

$$\text{Slew rate} = \alpha \ I/C$$

Where C is the total capacitance connected to the output node (this includes the compensation capacitor CC) and I is the current source current magnitude. Another important factor in the comparators design is the comparators resolution. The comparator needs to be able to distinguish voltage differences to within 1 LSB of accuracy, in this case 9.4 mV. The resolution of the comparator is determined by the gain of the comparator i.e. the gain of both stages. Increasing the current to increase the comparators response time also helps to improve the resolution at the expense of increased power consumption.

IV. Layout Design

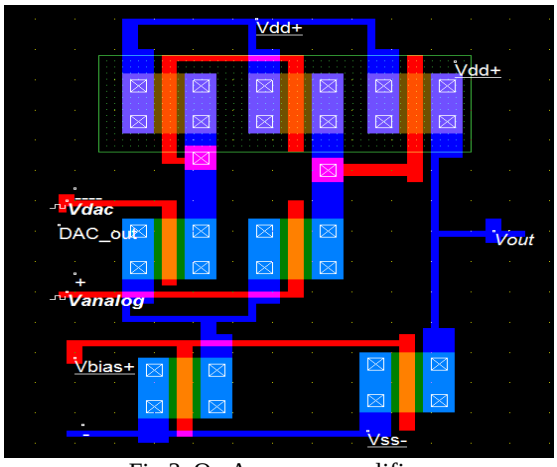

Fig.3. Op Amp s an amplifier

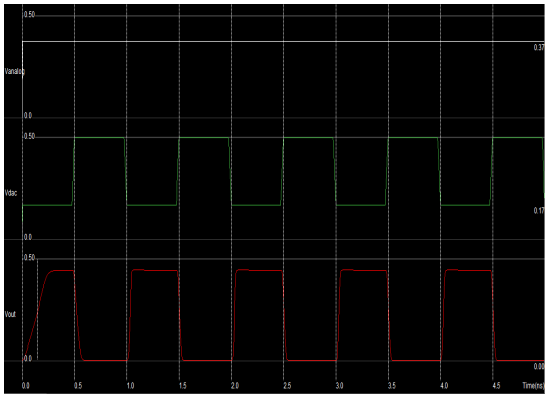

Fig.4. Timing Simulation of Op Amp s an amplifier

V. Regulation of Charge Pumps

In a charge pump, the output voltage has a linear dependence with respect to the load current, exhibiting an equivalent output resistance. In most applications, the output voltage should be kept constant under different load current. To achieve this, the regulated charge pump is use.

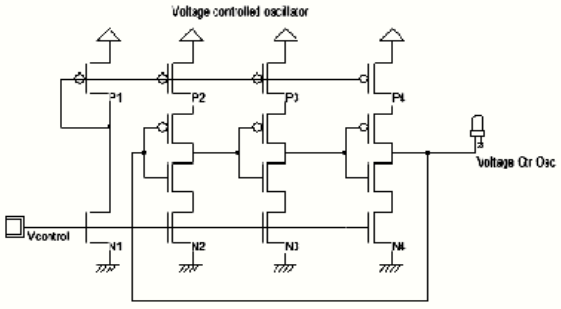

Fig.5. Schematic diagram of current starved voltage control oscillator.

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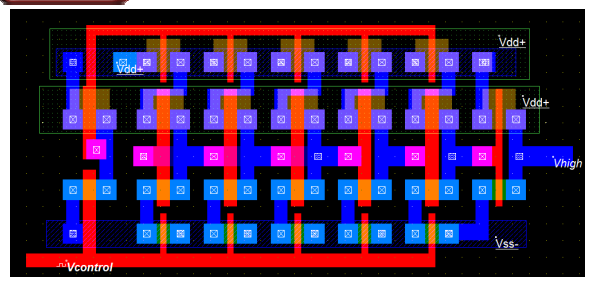

Fig.6. Voltage Control Oscillator

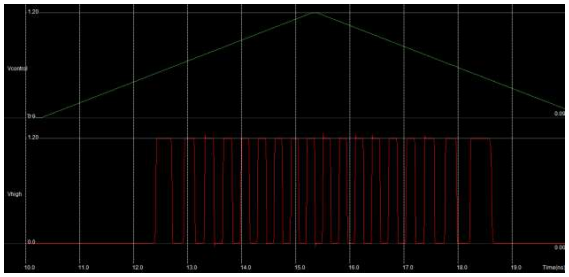
Fig.7. Timing Simulation of Voltage Control Oscillator

The regulation circuit uses a comparator to compare a fraction of the output voltage against a reference voltage. It employs a clock-blocking scheme to disable to input clock when the output voltage is higher than the desired voltage. By using this regulation scheme, a constant output voltage level can be achieved under different load currents. However, the circuit has to use an external clock and has a large ripple with high load currents. An internal clock can be generated by using a voltage-controlled oscillator (VCO) instead of using an external clock. If the output frequency of an oscillator can be varied by a voltage, then the circuit is called a "voltage controlled oscillator" (VCO). Due to the reduction of power consumption of digital circuit & the scaling of modern technologies, the supply voltage of integrated circuits continues to decreases. A CMOS VCO can be built using ring structure, relaxation circuits, or an LC resonant circuit. After the output voltage is detected, a bias voltage generation block compares a fraction of the output voltage with the reference voltage and adjusts the bias voltage for the VCO to produce the desired clock frequency.

VI. Result Analysis

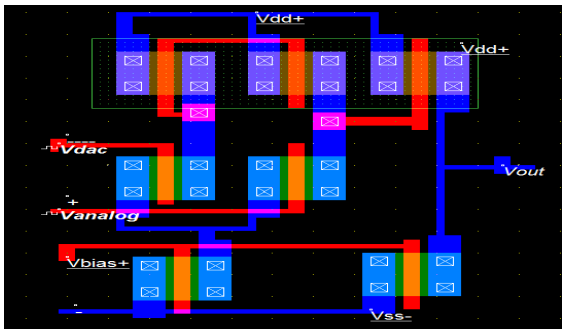

Fig.8. Differential Amplifier as Comparator

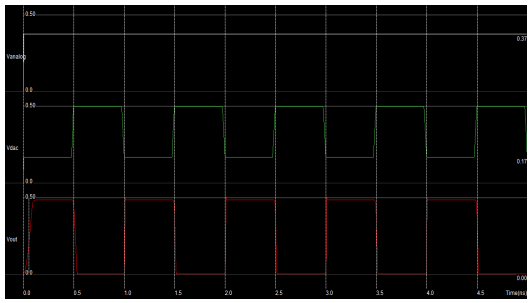
Fig.9. Timing Simulation of Differential Amplifier as Comparator

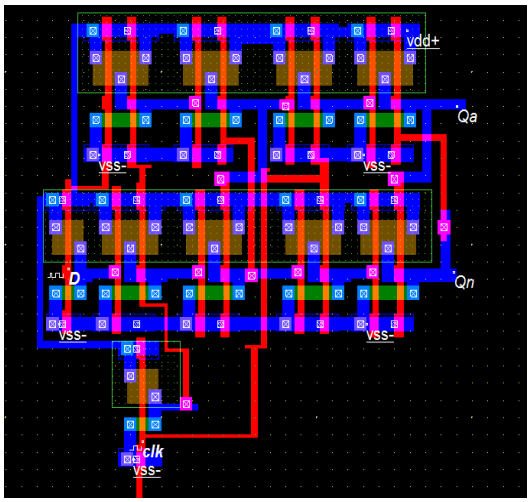

Fig.10. CMOS Layout design for D Flip-flop as phase Detector

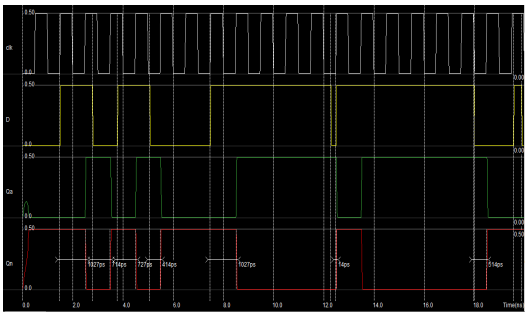
Fig.11. Timing Simulation of D Flip-flop as phase Detector

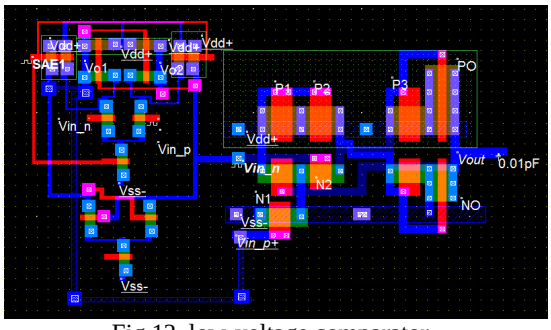

Fig.12. low-voltage comparator.

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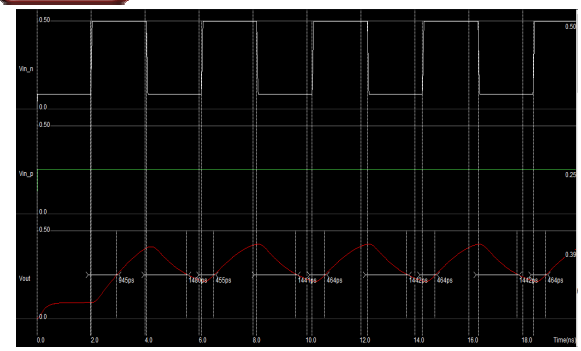

Fig.13. Timing Simulation of low-voltage comparator.

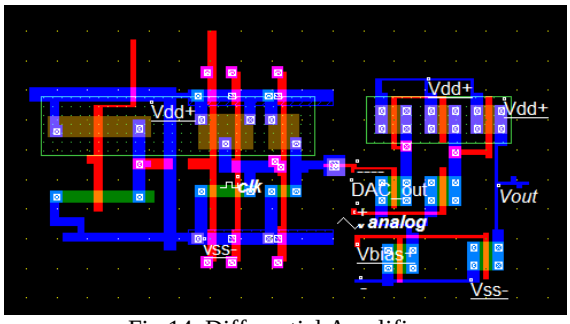

Fig.14. Differential Amplifier

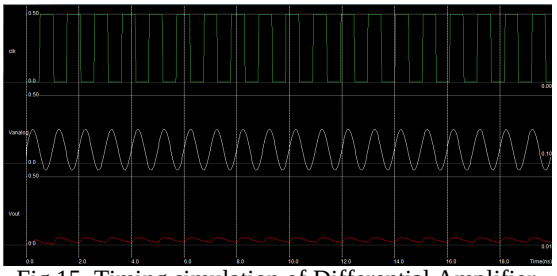

Fig.15. Timing simulation of Differential Amplifier

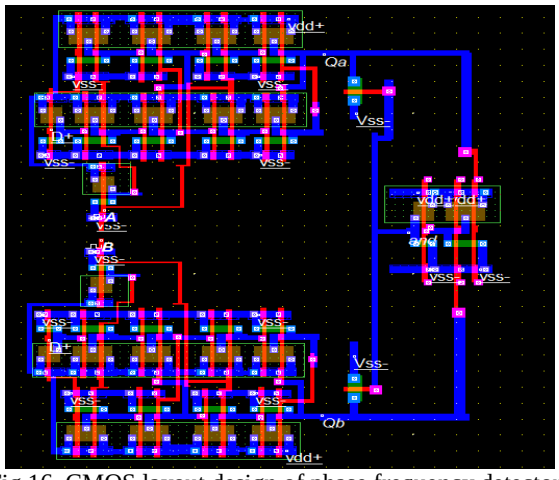

Fig.16. CMOS layout design of phase frequency detector.

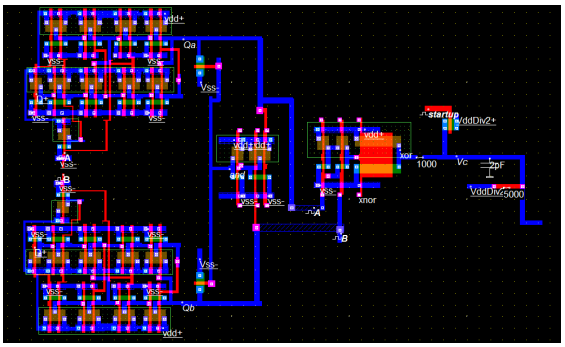

Fig.17. Low Voltage Reference Circuit using PFD and CPL

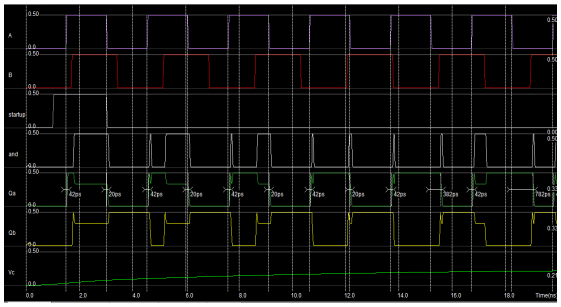

Fig.18. Timing Simulation of Low Voltage Reference Circuit using Phase frequency Detector and Charge Pump Logic.

Comparative Analysis

	[1] Byung-Do Yang	This Work
Process	110 nm	50nm
Area	13um	2.25um
Power Dissipation	5.35um	3.15um
Vref.	242mV	190mV

VII. CONCLUSION

The purpose of this work is design of low reference voltage generated stable DC to low and high voltage level converter circuit. A sub-threshold CMOS voltage reference circuit has been discussed. This circuit is based on the CMOS voltage reference circuit operating at a low supply voltage. Work is design of CMOS layout for low voltage comparator with an auxiliary amplifier structure. Auxiliary amplifier is design with two cross connected NMOS. The drain terminal of one NMOS is connected to the gate terminal of second NMOS in auxiliary amplifier structure. The voltage amplification on the nodes V01 and V02 by the cross coupled latch is very slow because the pull-down current of the cross-coupled latch is limited to the drain currents of both transistors It reduces the minimum required supply voltage by replacing the analog amplifier with the low-voltage comparator, charge-pump circuit, and digital control circuit. The architecture of the proposed charge pump is based on continuous current

pumping technique. In general, a charge pump is required to provide the load current, all the time. The input power supply should deliver enough charge during each clock cycle to fulfil the load current requirement. The reference voltage circuit is design in 50 nm CMOs technology. Its core area is 2.25um and it consumes 3.15uW power at 0.5V supply. The total number of transistors requires for design is 87.

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